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A fill-unit approach to multiple instruction issue - group of 4 »

M Franklin, M Smotherman - 27th Intl. Symp. on Microarchitecture, 1994 - portal acm.org ... The VLIW instruction format exactly represents the functionality and number of resources on a given im- ... together in one VLIW instruction ... Cited by 57 - Web Search

Instruction Scheduling for Clustered VLIW Architectures - group of 13 »

FJ Sanchez, A Gonzalez - ISSS, 2000 - doi.ieeecomputersociety.org

... VLIW Instruction ... employs a unified assign-and-schedule approach, as pro-posed by Özer et al. ... possible clus- ter (ie those clusters with an empty slot for the ...

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Flexible Issue Slot Assignment for VLIW Architectures - group of 4 »

Z Chamski, C Eisenbeis, E Rohou - RAPPORT DE RECHERCHE-INSTITUT NATIONAL DE RECHERCHE EN ..., 1999 - inria.fr

... the TriMedia, each VLIW instruction contains ve slots. In each of these ve slots, only some specied types of operations can take place. For instance, in slot 1 ... Cited by 7 - View as HTML - Web Search - BL Direct

Compiler optimization on VLIW instruction scheduling for low power - group of 5 »

C Lee, JK Lee, T Hwang, SC Tsai - ACM Transactions on Design Automation of Electronic Systems, 2003 portal.acm.org

... i and I i if microin- struction I i can be scheduled into the same position, or slot, in the whole VLIW instruction as the position of microinstruction u ... Cited by 12 - Web Search - BL Direct

Inter-Cluster Communication Models for Clustered VLIW Processors - group of 10 »

A Terechko, EL Thenaff, M Garg, JTJ Eijndhoven, H ... - HPCA, 2003 - ieeexplore.ieee.org ... lead to expansion of the VLIW in- struction, complicating the instruction decoder.

Moreover, this ICC model needs two extra RF ports per dedicated slot and the ... Cited by 18 - Web Search

Modulo scheduling for a fully-distributed clustered VLIW architecture - group of 10 »

J Sanchez, A Gonzalez - MICRO-ANNUAL WORKSHOP THEN ANNUAL INTERNATIONAL SYMPOSIUM-, 2000 portal.acm.org

... In the example, the VLIW instruction that contains the ... the number of cycles that the instruction stalls is ... the clusters in which there is an available slot. ... Cited by 35 - Web Search - BL Direct

Automatic generation of application specific processors - group of 3 »

D Goodwin, D Petkov - Proc. of Int'l Conf. on Compilers, Architecture, and ..., 2003 - portal acm.org ... Instruction Formats x24: size 24 bits, 1 slot slot Inst: size 24 ... Figure 3: Example configuration generated for SAD example for VLIW issue width of 1 and ... Cited by 23 - Web Search

Automatic Design of VLIW and EPIC Instruction Formats - group of 5 »

S Aditya, BR Rau, R Johnson - HP LABORATORIES TECHNICAL REPORT HPL, 2000 - fog.hpl.external.hp.com

... execution in a VLIW or EPIC processor ... We define the canonical instruction format

to be the MultiOp **instruction** format that has an ... ation **slot** per functional unit ... <u>Cited by 15 - View as HTML - Web Search - BL Direct</u>

A Configurable Platform for Advanced System-On-Chip Applications
R Priebe, C Ussery - Proc. Int'l Conf. Signal Processing Applications & ... - improvsys.com
... Instruction Word Configuration VLIW offers significant performance ... slots available
in the instruction for computation ... or more computation units into each slot. ...
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## [PS] Debugging VLIW code after instruction scheduling

LE Cool - 1992 - cse.ogi.edu

Page 1. Debugging **VLIW** Code After **Instruction** Scheduling by ... July 1992 Page 2. The thesis "Debugging **VLIW** Code After **Instruction** Scheduling" by Lyle Edward ... <u>Cited by 7 - View as HTML - Web Search</u>

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